Parallel Output (635-0752-001, -002)

Rockwell International

instructions

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1. DESCRIPTION

Parallel Output 635-0752-001, -002, shown in figure 1, is a 2-layer planar card with a 130-pin (2 layers, 65 pins each) edge-on connector. All test points are mounted at the top edge of the card for easy access with the card installed in the unit.

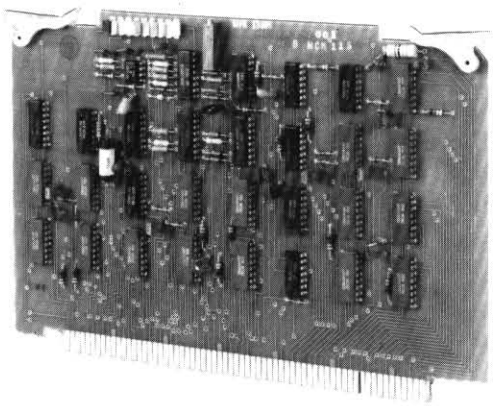
2. PRINCIPLES OF OPERATION

2.1 General

The parallel output card consists of 6 primary circuits: 16 shift registers used as multiplexers, 4 power-on-clear flip-flops, a strobe generator, an rf gain control, a fault indicator flasher, and an update/busy indicator/address gate (ADRG) generator. The multiplexers receive serial data and convert it to parallel outputs for application to front panel indicators. The rf gain control circuits are used only in the remote mode of the receiver circuits. A series of gates and flip-flops generates update, address gate, and busy indicator signals for use by control unit circuits. Outputs from the power-on-clear flip-flops momentarily set all the multiplexers to a no-output condition when power is initially applied to the circuits. A timing circuit develops a flashing signal for the R/E FAULT indicator under certain conditions.

2.2 Power-On-Clear

When power is applied to the parallel output card, capacitor C15 begins charging, through R28, to +5 volts. (Refer to the schematic diagram, figure 7.) Initial current through R28 develops a logic 1 voltage for approximately 1 second. When capacitor C15 is charged, no current flows through R28 and the voltage across R28 is logic 0. This momentary logic 1



TP5-2313-017

Parallel Output
Figure 1

NOTICE: This section replaces first edition dated 1 June 1977.

is applied to the set terminals of flip-flops U5A and B, and U17A and B. The flip-flop $\overline{Q}$ outputs at logic 0 with set state are applied to the enable lines of the 16 shift register multiplexers. This clears all the multiplexer outputs to an initial open-circuit condition.

2.3 Serial-to-Parallel Register

The 16 shift registers are electronically arranged in 4 groups of 4. Each group of shift registers represents one word, each shift register represents one character of the word, and each register output represents one of the eight data bits of the word. (This information is shown in detail in the columns to the right of the shift registers in the schematic diagram, figure 7.)

When the local enable (LOCAL EN) signal at P1-16 is logic 1, the enable (EN) input to all the shift registers is logic 0 which inhibits their operation. (Figure 2 shows a truth table and block diagram of the type 4094 shift register.) A logic 0, or open circuit pulled down to logic 0 by R30, at P1-16 permits the shift registers to be enabled. In this condition, the data input (P1-89) is applied to the character-5 register of each word group. The clock input (P1-88) clocks the data serially through each of the registers in a word group. When all 8 bits of characters 2 through 4 are loaded, a strobe signal at the register strobe inputs will cause the data to be stored in the registers. (Refer to the shift register block diagram in figure 2.) With the enable inputs at logic 1, the stored data is applied through buffers to the eight outputs of the shift registers. This is the parallel output signal from the circuit card.

Strobe signals to each of the word groups of registers are generated by U7. Outputs from this 8-channel multiplexer (refer to the block diagram and truth table in figure 3) are determined by the inputs to the A and B control inputs (P1-83 and -81), the strobe addresses (STA 1 and STA 2) from the serial interface card. The output signals from U7 strobe one word group of registers at a time to output the word data bits from the registers.

2.4 Fault Indicator Flasher

A type 4047 multivibrator (refer to figure 4) is connected as a retriggerable astable multivibrator to develop an on-off signal to the unit front panel R/E FAULT indicator.

During normal operation, the strobe signal to the U8 retrigger input occurs at a rate that keeps the astable multivibrator continuously triggered ($\overline{Q}$ at logic 0). This permits bit 1 of character 4, word 4 to control the output of exclusive OR gate U12B. If this character bit is logic 0, the r/t fault ind signal at P1-12 is logic 1 and the unit front panel R/E FAULT indicator is turned on. Otherwise, the output is logic 0 and the indicator is off.

In the event a malfunction interrupts monitor data transmission between the control and remote units (interconnection interruption or serial interface card malfunction, for example) the strobe signal to the U8 retrigger input goes to logic 0. This allows the multivibrator to free run at a 0.25-Hz rate (logic 1, 2s, logic 0, 2s). Regardless of the logic level at U12B-5, the r/t fault ind output will be pulsed between logic 1 and 0 to cause the R/E FAULT indicator to flash.

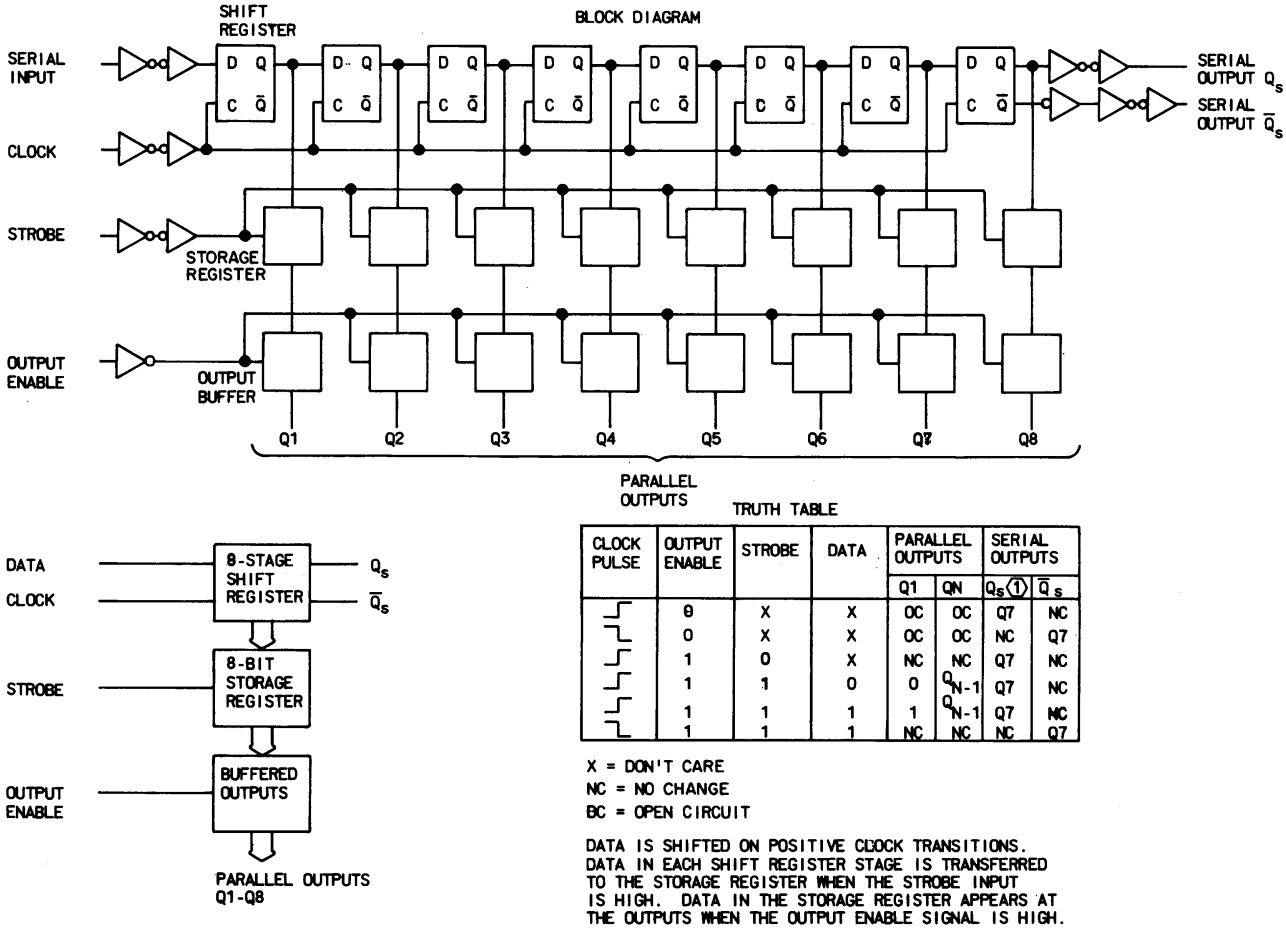
2.5 RF Gain Control

The rf gain control circuit develops a dc voltage output proportional to the binary input signals to multiplexers U2 and U10. Input signals to the multiplexers are obtained from serial-to-parallel shift register U10. The various dc output levels are developed by changing the input resistors to U1A. This is done by enabling different outputs from U10 or U2. The enabled output channel of the multiplexer is determined by the binary signals at the control inputs (pins A, B, and C). (Refer to figure 3 for a truth table and block diagram of the type 4051 multiplexer.)

When the inhibit (INH) input to the multiplexer is logic 1, the outputs are all open circuit. In local mode of operation of the remote units, the local enable input to NOR gates U9A (pin 1) and U9B (pin 5) is strapped to logic 1. This inhibits the operation of both U2 and U10 and applies approximately 0 volt to P1-86 (remote rf gain control). Otherwise, in the remote mode of operation, these inputs to U9A and B are at logic 0. The rf gain (16) signal is logic 0; this causes multiplexer U10 to be enabled and U2 to be inhibited. When the rf gain level is adjusted to the point where rf gain (16) signal goes to logic 1, U10 is inhibited and U2 is enabled (through inverter U2). Thus the various input resistor values are selected to control the dc output level from amplifiers U1A and U1B.

2.6 Update/Busy Indicator/Address Gate Generator

This circuit consists of gates U4; U12A, C, and D; U28; inverters U11A, B, and F; flip-flops U20 (truth table and diagram in figure 5); and multivibrators U3 (diagram and waveforms in figure 6). The circuit



TRUTH TABLE

CLOCK PULSE	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	Q_s ①	$\overline{Q}_s$
⌐	0	X	X	OC	OC	Q7	NC
⌐	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌐	1	1	1	NC	NC	NC	Q7

X = DON'T CARE
NC = NO CHANGE
BC = OPEN CIRCUIT

DATA IS SHIFTED ON POSITIVE CLOCK TRANSITIONS. DATA IN EACH SHIFT REGISTER STAGE IS TRANSFERRED TO THE STORAGE REGISTER WHEN THE STROBE INPUT IS HIGH. DATA IN THE STORAGE REGISTER APPEARS AT THE OUTPUTS WHEN THE OUTPUT ENABLE SIGNAL IS HIGH.

NOTES:
① AT THE POSITIVE CLOCK EDGE, INFORMATION IN THE 7TH SHIFT REGISTER IS TRANSFERRED TO THE 8TH REGISTER STAGE AND THE Q_s OUTPUT.

TP5-2028-013

8-Stage Shift-and-Store Bus Register CD4094BE
Figure 2

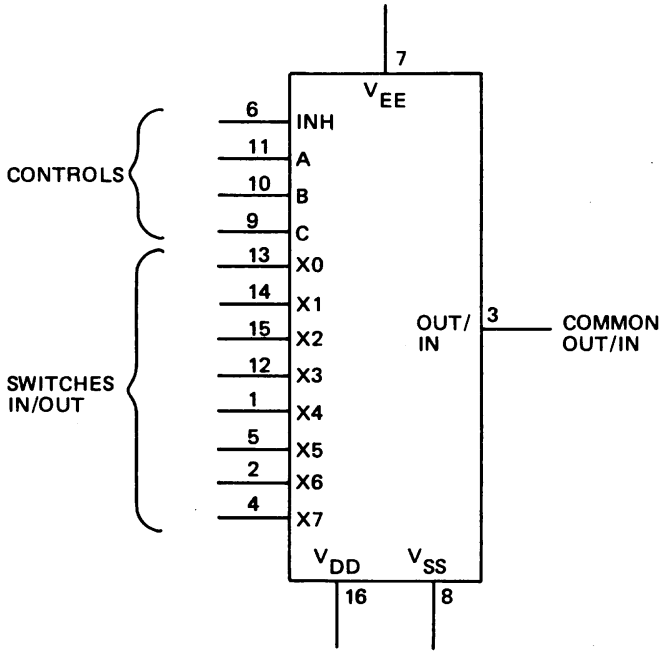
develops address gate and update pulses, and a driving voltage for the unit front panel BUSY indicator. (These signals are used in the control unit only.)

With the unit front panel CONT switch in NORM and no busy signal input from the unit being controlled, the input to U4D-13 is logic 0. The input from P1-71 through U11B to U4D-12 is logic 1. This develops a logic 0 from exclusive OR gate U12D and AND gate U28B. The logic 0 U28B output prevents the BUSY indicator on the unit front panel from lighting. This same signal is clocked through U20A to inhibit U28D from gating out WD4R pulses which are used as update requests.

When a busy signal input is received in the monitor data, the input to U4D-13 goes to logic 1. In NORM, U4D-11 is logic 0, U12D-11 is logic 1, and both inputs to U28B are logic 1. This develops a logic 1 to U28A-2 and to busy indicator output (to cause the BUSY indicator to light). The input to U28A from U4D-11 enables U28A and causes it to output continuous WD4R pulses as an address gate signal. The input to U28C-8 is logic 0, causing gate U28D to keep the update output inhibited.

When the front panel CONT switch is changed from NORM to TEST in a not-busy condition, U4D-13 is logic 0 keeping the busy indicator output at logic 0 as

SYMBOL

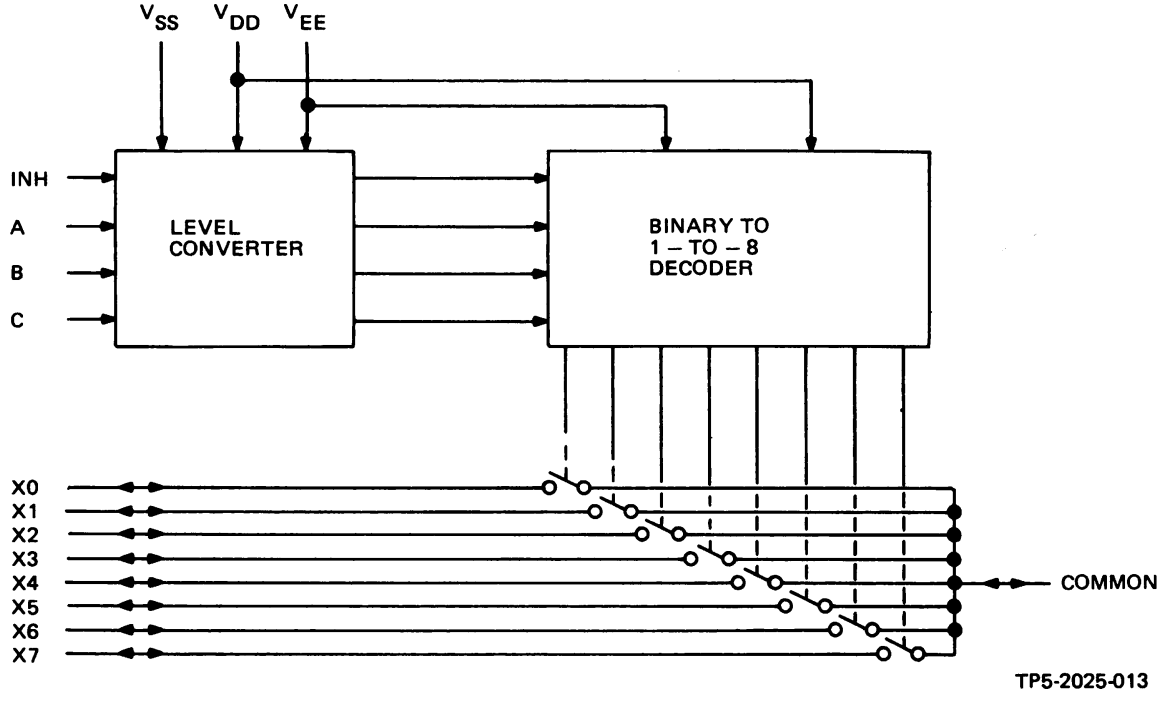


TRUTH TABLE

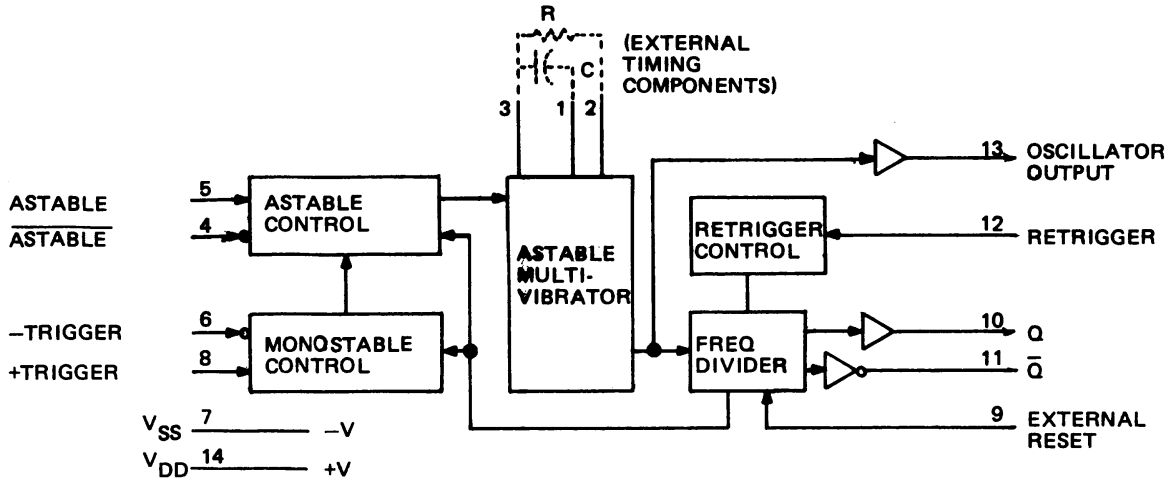
CONTROL				CLOSED SWITCH (COMMON)
INH	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	X	X	X	NONE

X = DON'T CARE

FUNCTIONAL DIAGRAM



8-Channel Multiplexer/Demultiplexer MC14051B
Figure 3



FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3, EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3.

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
ASTABLE MULTIVIBRATOR:					
FREE RUNNING	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	t_A (10, 11)=4.40 RC
TRUE GATING	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A (13)=2.20 RC
COMPLEMENT GATING	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
MONOSTABLE MULTIVIBRATOR					
POSITIVE-EDGE TRIGGER	4, 14	5, 6, 7, 9, 12	8	10, 11	
NEGATIVE-EDGE TRIGGER	4, 8, 14	5, 7, 9, 12	6	10, 11	
RETRIGGERABLE	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10, 11)=2.48 RC

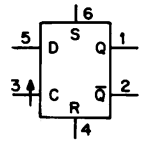
TP5-2029-012

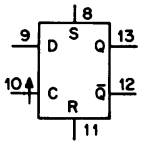
Low-Power Monostable/Astable Multivibrator CD4047AE
Figure 4

before. (The logic 0 input to U28A also keeps the ADRG output inhibited.) Switching from NORM to TEST causes U12C to develop a momentary output pulse that is used to trigger U3A. The resulting output from U3B is a logic 1 pulse that causes a logic 0 output from U4A-3. This input to U12A allows the exclusive OR gate to momentarily go to logic 1 and set U20A-1 to logic 1. (The not-busy, logic 0 input from U28B-4 to U20A-5 and clock input to U20A-3 from the WD4R clock the Q output from U20A-1 back to logic 0.) The momentary logic 1 at U28D-13 permits one WD4R pulse to be gated out (U28D-11) as an update pulse.

With a busy signal present (U4D-13 at logic 1) when the CONT switch is placed in the TEST position, the set pulse to U20A-6 is developed as described above; however, the resulting logic 1 from U4D-11 causes U12D-11 to be logic 0. This switches the logic 1 busy indicator output to logic 0, turning off the front panel busy indicator, and causes the Q output from U20A to go to logic 0 after the set input pulse from U12A goes to logic 0. The resulting update output is one logic 1 pulse and the ADRG output is a constant logic 0.

When the front panel CONT switch is changed from TEST to NORM, the logic 1 output pulse from U3B-10





V_{DD} = 14
V_{SS} = 7

TRUTH TABLE

INPUTS				OUTPUTS	
CLOCK*	DATA	RESET	SET	Q	$\overline{Q}$
⌐‾	0	0	0	0	1
⌐‾	1	0	0	1	0
‾⌐	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

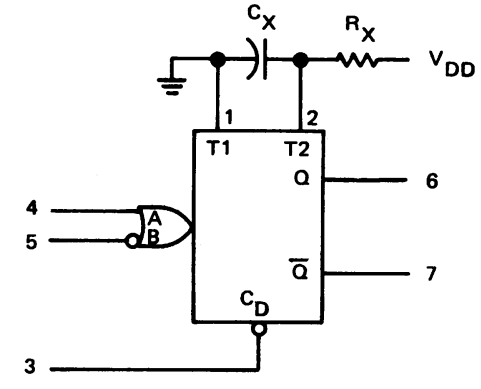
NO CHANGE

X = DON'T CARE
* = LEVEL CHANGE

TP5-2027-012

Dual D-Type Flip-Flop CD4013AE
Figure 5

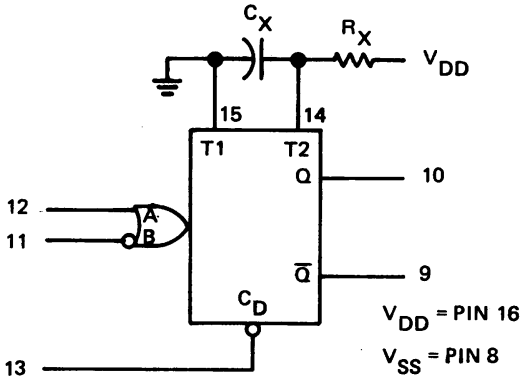
BLOCK DIAGRAM



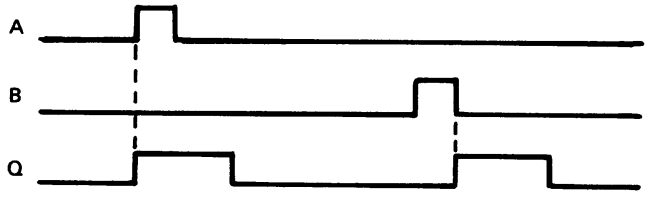
A INPUT TERMINAL CLOCKS ON 0-TO-1 TRANSITION.

B INPUT TERMINAL CLOCKS ON 1-TO-0 TRANSITION.

C_D (RESET) TERMINAL, WHEN SWITCHED TO LOGIC 0, IMMEDIATELY TERMINATES OUTPUT PULSE.



R_X AND C_X ARE EXTERNAL COMPONENTS.



TP5-2299-011

Dual Monostable Multivibrator CD4098BE
Figure 6

is developed as described above. (Exclusive OR gate U12C develops an output trigger pulse to U3A-4 when the input to pin 8 changes from one logic level to the other.) With a not-busy signal present, U4D-11 is logic 1. This enables U28C to gate the WD4R pulses to U28D. The logic 1 at U12D-13 develops a logic 0 at U12D-11 and inhibits gate U28B. The logic 0 output from U28B-4 is the busy indicator output, the D input to U20A, and an inhibiting input to U28A. The resulting Q output from U20A inhibits gate U28D, developing a logic 0 update output. With U28A inhibited, the ADRG output is also held at logic 0.

With a busy signal present when the CONT switch is set to NORM, U4D-11 is logic 0 which causes the update output to be logic 0. The logic 1 output from U12D-11 causes U28B-4 to be switched to logic 1. This outputs a logic 1 busy indicator signal and enables gate U28A. The WD4R input to U28A-1 is then gated out as continuous ADRG pulses.

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the parallel output card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 1 check total performance of the parallel output card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 1. Parallel Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	**Note** These testing and troubleshooting procedures are based on using a control unit and an associated local unit. The most effective method of testing and troubleshooting is obtained by installing the questionable parallel output in the control unit. During these tests when a control unit is referred to it is a receiver-exciter control, or a receiver control. When a local unit is referred to it is a receiver-exciter, an exciter, or a receiver.		
	a. Remove top cover of unit containing the parallel output that is to be tested.		
	b. Remove parallel output. Install it on an extender card and place it in the control unit.		
	c. Set control unit and local unit LINE SELECTOR switches to 115 V.		
	d. Connect control unit and local unit to 115-V ac power source and set power on.		
	e. Measure dc voltages, on the card under test, between the following pins and ground (TP1, brown):		
	P1-45 P1-65 P1-114	+15 ±1.0 V dc. +5 ±0.5 V dc. -15 ±1.0 V dc.	Check associated power supply.
	f. Strap local unit for address 0.		
	g. Connect local unit to control unit.		
2. Data inputs, word 1	a. Set control unit CONT switch to TEST. **Note** Word 1 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in LCL. Then set local unit controls to positions indicated.		
(Cont)	b. Set control unit FREQUENCY KHZ controls for 29 999.9(9).	Frequency display reads 29 999.9(9). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. Data inputs, word 1 (Cont)	c. Set control unit FREQUENCY KHZ controls for 16 666.6(6).	Frequency display reads 16 666.6(6). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	d. Set control unit FREQUENCY KHZ controls for 02 000.0(0).	Frequency display reads 02 000.0(0). Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
10 MHz	(2)	129	1	0	0	U6, U5, U7, U11, and associated circuits.
	(1)	64	0	1	0	
1 MHz	(8)	128	1	0	0	
	(4)	63	0	1	0	
	(2)	127	0	1	1	
	(1)	62	1	0	0	
100 kHz	(8)	126	1	0	0	U14, U5, U7, U11, and associated circuits.
	(4)	61	0	1	0	
	(2)	125	0	1	0	
	(1)	60	1	0	0	
10 kHz	(8)	124	1	0	0	
	(4)	59	0	1	0	
	(2)	123	0	1	0	
	(1)	58	1	0	0	

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

2. Data inputs, word 1 (Cont)

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS 29 999.9(9)	16 666.6(6)	02 000.0(0)	IF ABNORMAL CHECK
1 kHz	(8)	122	1	0	0	U22, U5, U7, U11, and associated circuits.
	(4)	57	0	1	0	
	(2)	121	0	1	0	
	(1)	56	1	0	0	
100 Hz	(8)	120	1	0	0	
	(4)	55	0	1	0	
	(2)	119	0	1	0	
	(1)	54	1	0	0	
10 Hz (with no 10-Hz tuning)	(8)	118	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	53	0	0	0	
	(2)	117	0	0	0	
	(1)	52	0	0	0	
10 Hz (with 10-Hz tuning)	(8)	118	1	0	0	
	(4)	53	0	1	0	
	(2)	117	0	1	0	
	(1)	52	1	0	0	
1 Hz (with no 1-Hz tuning)	(8)	116	0	0	0	U30, U5, U7, U11, and associated circuits.
	(4)	51	0	0	0	
	(2)	115	0	0	0	
	(1)	50	0	0	0	
1 Hz (with 1-Hz tuning)	(8)	116	1	0	0	
	(4)	51	0	1	0	
	(2)	115	0	1	0	
	(1)	50	1	0	0	

Note

If a processor control is used, the 1-Hz outputs can be checked in the same manner that the other frequency outputs are checked.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)	a. Set control unit CONT switch to TEST. **Note** Word 2 tests can also be accomplished with the control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit or control unit parallel output card (the card being tested). Rf gain test, steps b and c, is applicable to receiver and receiver-exciter controls only. b. Set control unit RF GAIN control to MAX. c. Connect a dvm to TP5 (green).	Note dc levels as shown in chart for different RF GAIN positions.	Check U18, U9, U11, U1, and associated circuits. Check also circuit indicated in chart.

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	1	0.000 ±0.010	None
↓	*	-0.158 ±0.010	R20
	2	-0.316 ±0.010	R19
	*	-0.475 ±0.020	R19, R20
	3	-0.634 ±0.020	R18
	*	-0.792 ±0.030	R18, R20
rotated	4	-0.950 ±0.030	R17
from MAX	*	-1.108 ±0.040	R17, R20
ccw toward	5	-1.266 ±0.040	R16
MIN	*	-1.417 ±0.050	R16, R20
↓	6	-1.568 ±0.050	R15
	*	-1.712 ±0.060	R15, R20
	7	-1.855 ±0.060	R14
	*	-2.022 ±0.070	R14, R20
	8	-2.188 ±0.070	R13
MIN	*	-2.332 ±0.080	R13, R20

and U10.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

RF GAIN CONTROL SETTINGS		TP5 (DC VOLTS)	IF ABNORMAL CHECK
MAX	9	-2.465 ±0.080	R12
↓	*	-2.619 ±0.090	R12, R20
	10	-2.773 ±0.090	R11
	*	-3.002 ±0.100	R11, R20
	11	-3.130 ±0.100	R10
	*	-3.283 ±0.110	R10, R20
rotated	12	-3.439 ±0.110	R9
from MAX	*	-3.570 ±0.120	R9, R20
ccw toward	13	-3.700 ±0.120	R8
MIN	*	-3.886 ±0.130	R8, R20
	14	-4.072 ±0.130	R7
↓	*	-4.218 ±0.140	R7, R20
	15	-4.363 ±0.140	R6
	*	-4.532 ±0.150	R6, R20
	16	-4.700 ±0.150	R5
MIN	*	-4.858 ±0.160	R5, R20

} and U2.

*Controlled by least significant bcd input for rf gain control, available only on processor controls. Bcd for least significant bcd signal at MAX setting is bit wt 0. Bcd signal for most significant bcd signal at one step beyond MIN setting is bit wt 31.

Note

AGC tests, steps d through f, are applicable to the receiver and receiver-exciter controls only.

(Cont)	d. Set control unit AGC switch to FAST.	Check logic levels at the associated parallel output pin numbers as shown in chart.
	e. Set control unit AGC switch to OFF.	Check logic levels at the associated parallel output pin numbers as shown in chart.
	f. Set control unit AGC switch to SLOW.	Check logic levels at the associated parallel output pin numbers as shown in chart.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. Data inputs, word 2 (Cont)

(Cont)</td><td>
Note
Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="3">AGC SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>FAST</th><th>OFF</th><th>SLOW</th></tr>
<tr><td>CH A AGC OFF</td><td>84</td><td>0</td><td>1</td><td>0</td><td rowspan="4">U26, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>CH A AGC FAST</td><td>85</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>CH B AGC OFF</td><td>19</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>CH B AGC FAST</td><td>20</td><td>1</td><td>0</td><td>0</td></tr>
</table>
Note
Bandwidth tests, steps g and h, are applicable to the receiver control only.

g. Set control unit MODE switch to SSB/CW.

h. Set control unit BANDWIDTH switch to each of its positions.

Note
Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.
</td><td>The display associated with the BANDWIDTH switch positions lights. Refer to chart for logic levels and associated parallel output pin numbers.</td><td>Measure logic levels as indicated in chart.</td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Data inputs, word 2 (Cont)			

PARALLEL OUTPUT	PIN NO P1-( )	BANDWIDTH SWITCH POSITION								IF ABNORMAL CHECK
		16	A	B	USB	LSB	C	D	E	
FL8	100	1	0	0	0	0	0	0	0	U27, U17, U7, U11, and associated circuits.
FL3	33	0	1	0	0	0	0	0	0	
FL4	98	0	0	1	0	0	0	0	0	
FL1	32	0	0	0	1	0	0	0	0	
FL2	97	0	0	0	0	1	0	0	0	
FL5	34	0	0	0	0	0	1	0	0	
FL6	35	0	0	0	0	0	0	1	0	
FL7	99	0	0	0	0	0	0	0	1	

Note

Mode tests, step i, are applicable to the receiver control only.

i. Set MODE switch (receiver control only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Measure logic levels as indicated in chart.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

3. Data inputs, word 2 (Cont)

PARALLEL OUTPUT	PIN NO P1-( )	MODE SWITCH POSITION			IF ABNORMAL CHECK
		*SSB/CW	*AM	ISB	
SSB EN	72	1	0	1	U25, U17, U7, U11, and associated circuits.
AM EN	8	0	1	0	
FM EN	73	0	0	0	
CW EN	9	0	0	0	
ISB EN	74	0	0	1	

*In these positions the display and logic levels associated with the BANDWIDTH switch position are also activated.

Note

Mode tests, step j, are applicable to the exciter and receiver-exciter controls only.

j. Set MODE switch (exciter and receiver-exciter controls only) to each of its positions.

The display associated with the MODE switch position lights. Refer to chart for logic levels and associated parallel output pin numbers.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.

(Cont)

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>3. Data inputs, word 2 (Cont)</td><td colspan="3">
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="5">MODE SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>CW</th><th>LSB</th><th>USB</th><th>AM</th><th>ISB</th></tr>
<tr><td>SSB EN</td><td>72</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="5">U25, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>AM EN</td><td>8</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>FM EN</td><td>73</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>CW EN</td><td>9</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>ISB EN</td><td>74</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>FL1 (USB) EN</td><td>32</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="2">U27, U17, U7, U11, and associated circuits.</td></tr>
<tr><td>FL2 (LSB) EN</td><td>97</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>4. Data inputs, word 3

(Cont)</td><td>a. Set control unit CONT switch to TEST.

Note

Word 3 tests can also be accomplished with control unit CONT switch in NORM and local unit CONT switch in REM. Then measure voltages at local unit parallel output card (the card being tested).

Pa tests, steps b through e, are applicable to the exciter and receiver-exciter controls only.

b. Set control unit PA PWR switch to OFF.

c. Set control unit PA PWR switch to STBY.

d. Set control unit PA PWR switch to HIGH PWR.</td><td>Check logic levels at the associated parallel output pin numbers as shown in chart.

Check logic levels at the associated parallel output pin numbers as shown in chart.

Check logic levels at the associated parallel output pin numbers as shown in chart.</td><td></td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>4. Data inputs, word 3 (Cont)</td><td>e. Set control unit PA PWR switch to LOW PWR.

Note

Logic 1 = NLT +3.0 V dc.
Logic 0 = NMT 0.5 V dc.</td><td>Check logic levels at the associated parallel output pin numbers as shown in chart.</td><td></td></tr>
<tr><td></td><td>
<table>
<tr><th rowspan="2">PARALLEL OUTPUT</th><th rowspan="2">PIN NO P1-( )</th><th colspan="4">PA PWR SWITCH POSITION</th><th rowspan="2">IF ABNORMAL CHECK</th></tr>
<tr><th>OFF</th><th>STBY</th><th>HIGH PWR</th><th>LOW PWR</th></tr>
<tr><td>PA LV EN</td><td>79</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="3">U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>PA HV EN</td><td>14</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>LO PWR EN</td><td>78</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td></td><td>Note

Pilot carrier tests, steps f and g, are applicable to the exciter and receiver-exciter controls only.

f. Set control unit P CAR switch to OFF.

g. Set control unit P CAR switch to ON.</td><td>Logic level 0 at P1-82 (NMT 0.5 V dc).

Logic level 1 at P1-82 (NLT +3.0 V dc).</td><td>Check U19, U5, U7, U11, and associated circuits.</td></tr>
<tr><td>(Cont)</td><td>Note

Dvbfo tests, steps h through k, are applicable only to the receiver and receiver-exciter controls with a dvbfo option installed.

h. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR.</td><td></td><td></td></tr>
</table>

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Data inputs, word 3 (Cont)	i. Set digital VBFO controls for +9990 Hz.	VBFO frequency display reads +9990. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	j. Set digital VBFO controls for -6660 Hz.	VBFO frequency display reads -6660. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	k. Set digital VBFO controls for +1000 Hz.	VBFO frequency display reads +1000. Refer to chart for logic levels and associated parallel output pin numbers.	Measure logic levels as indicated in chart.
	Note Logic 1 = NLT +3.0 V dc. Logic 0 = NMT 0.5 V dc.		
(Cont)			

BCD OUTPUT SIGNAL		PARALLEL OUTPUT PIN NO P1-( )	LOGIC LEVELS +9990	LOGIC LEVELS -6660	LOGIC LEVELS +1000	IF ABNORMAL CHECK
DVBFO 1 kHz	(8)	48	1	0	0	U29, U5, U7, U11, and associated circuits.
	(4)	113	0	1	0	
	(2)	47	0	1	0	
	(1)	112	1	0	1	
DVBFO 100 Hz	(8)	46	1	0	0	U21, U5, U7, U11, and associated circuits.
	(4)	111	0	1	0	
	(2)	110	0	1	0	
	(1)	44	1	0	0	
DVBFO 10 Hz	(8)	109	1	0	0	
	(4)	43	0	1	0	
	(2)	108	0	1	0	
	(1)	42	1	0	0	
DVBFO SIGN		107	1	0	1	U29, U5, U7, U11, and associated circuits.

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Data inputs, word 3 (Cont)	**Note** Analog vbfo tests, steps l and m, are applicable only to the receiver and receiver-exciter controls with an analog vbfo option installed. l. Set the control unit MODE switch to SSB/CW or CW and BFO switch to VAR. m. Rotate the BFO control through its complete range.	Check logic levels at the associated parallel output pin numbers as shown in chart.	

BCD OUTPUT SIGNAL		LOGIC LEVELS — PARALLEL OUTPUT PIN NO P1-( ) 48	113	47	112	LOGIC DISPLAY	IF ABNORMAL CHECK
- (Full ccw)	1	1	1	1	1		U29, U5, U7, U11, and associated circuits.
	2	1	1	1	0		
	3	1	1	0	1		
	4	1	1	0	0		
	5	1	0	1	1		
	6	1	0	1	0		
	7	1	0	0	1		
Rotated from - cw toward +	8	1	0	0	0		
	9	0	1	1	1		
	10	0	1	1	0		
	11	0	1	0	1		
	12	0	1	0	0		
	13	0	0	1	1		
	14	0	0	1	0		
	15	0	0	0	1		
+ (Full cw)	16	0	0	0	0		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4	a. Set control unit CONT switch to NORM.		
	b. Set local unit CONT switch to LCL.		
	Note		
	System key test, steps c and d, is applicable only to exciter and receiver-exciter controls.		
	c. Set local unit KEY switch to LOCK.	Control unit KEY display lights. Logic level 1 at P1-68 (NLT +3.0 V dc).	Check U15, U17, U7, U11, and associated circuits.
	d. Set local unit KEY switch to NORM.	Control unit KEY display goes out. Logic level 0 at P1-68 (NMT 0.5 V dc).	
	e. Set local unit PWR switch off and back on.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT lights. Logic level 1 at P1-12 (NLT +3.0 V dc).	Check U16, U12, U8, U17, U7, U11, and associated circuits.
	f. Change any frequency control on local unit front panel.	Control unit EXCTR FAULT, RCV FAULT, or R/E FAULT goes out. Logic level 0 at P1-12 (NMT 0.5 V dc).	
	Note		
	Receive overload test, steps g and h, is applicable only to receiver and receiver-exciter controls.		
	g. Connect +5 V dc to local unit J16-27.	Control unit RCV OVERLOAD lights. Logic level 1 at P1-67 (NLT +3.0 V dc)	Check U16, U17, U7, U11, and associated circuits.
	h. Remove +5 V dc from local unit J16-27.	Control unit RCV OVERLOAD goes out. Logic level 0 at P1-67 (NMT 0.5 V dc).	Same as step g.
	Note		
(Cont)	Coupler fault test, steps i and j, is applicable only to exciter and receiver-exciter controls.		

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4 (Cont)	i. Connect +5 V dc to local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 1 at P1-13 (NLT +3.0 V dc).	
	j. Remove +5 V dc from local unit J15-1.	Control unit COUPLER FAULT lights. Logic level 0 at P1-13 (NMT 0.5 V dc).	
	Note Rf out test, steps k and l, is applicable only to exciter and receiver-exciter controls.		
	k. Connect ground signal to local unit J15-5.	Control unit RF OUT lights. Logic level 1 at P1-5 (NLT +3.0 V dc).	
	l. Remove ground signal from local unit J15-5.	Control unit RF OUT goes out. Logic level 0 at P1-5 (NMT 0.5 V dc).	Same as step g.
	Note Pa fault test, steps m and n, is applicable only to exciter and receiver-exciter controls.		
	m. Connect +5 V dc to local unit J15-3.	Control unit PA FAULT lights. Logic level 1 at P1-77 (NLT +3.0 V dc).	
	n. Remove +5 V dc from local unit J15-3.	Control unit PA FAULT goes out. Logic level 0 at P1-77 (NMT 0.5 V dc).	
	Note Pa ready test, steps o and p, is applicable only to exciter and receiver-exciter controls.		
(Cont)	o. Connect ground signal to local unit J15-21.	Control unit PA READY lights. Logic level 0 at P1-69 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data Inputs, word 4 (Cont)	p. Remove ground signal from local unit J15-21.	Control unit PA READY goes out. Logic level 0 at P1-69 (NMT 0.5 V dc).	Same as step g.
	q. Press and hold local unit CONT switch to MON.	Logic level 1 at P1-30 (NLT +3.0 V dc).	Check U24, U17, U7, U11, and associated circuits.
	r. Set local unit CONT switch to REM.	Logic level 0 at P1-30 (NMT 0.5 V dc).	
	s. Set local unit CONT switch to LCL.	Logic level 1 at P1-95 (NLT +3.0 V dc).	
		Control unit BUSY indicator lights. Logic level 1 at P1-7 (NLT +3.0 V dc).	Check U28, U20, U12, U4, U24, U17, U7, U11, and associated circuits.
	t. Set local unit CONT switch to REM.	After short delay logic level 0 at P1-95 (NMT 0.5 V dc).	Same as step s.
		After short delay control unit BUSY indicator goes out. Logic level 0 at P1-7 (NMT 0.5 V dc).	
	u. Set local unit CONT switch to LCL.		
	v. Apply a ground to local unit A13U51A-6.		
	w. Apply a ground to local unit A13U51A-3.		
	x. Remove ground from local unit A13U51A-3.		
	y. Apply ground to local unit A13U16A-1, 2, 8.		
	z. Remove ground from local unit A13U16A-1, 2, 8.	Logic level 1 at P1-29 (NLT +3.0 V dc).	Same as step q.
	aa. Remove ground from local unit A13U51A-6.		
(Cont)	ab. Apply ground to local unit A13U42A-3.	Logic level 0 at P1-29 (NMT 0.5 V dc).	

Table 1. Parallel Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Data inputs, word 4 (Cont)	ac. Remove ground from local unit A13U42A-3. **Note** Preselector fault tests, steps ad and ae, are applicable to receiver and receiver-exciter controls only.		
	ad. Apply +5 V dc to local unit J16-8.	Control unit PRESEL FAULT lights. Logic level 1 at P1-28 (NLT +3.0 V dc).	Same as step q.
	ae. Remove +5 V dc from local unit J16-8.	Control unit PRESEL FAULT goes out. Logic level 0 at P1-28 (NMT 0.5 V dc).	

4. REPAIR

Repair of the parallel output card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

5. PARTS LIST/DIAGRAMS

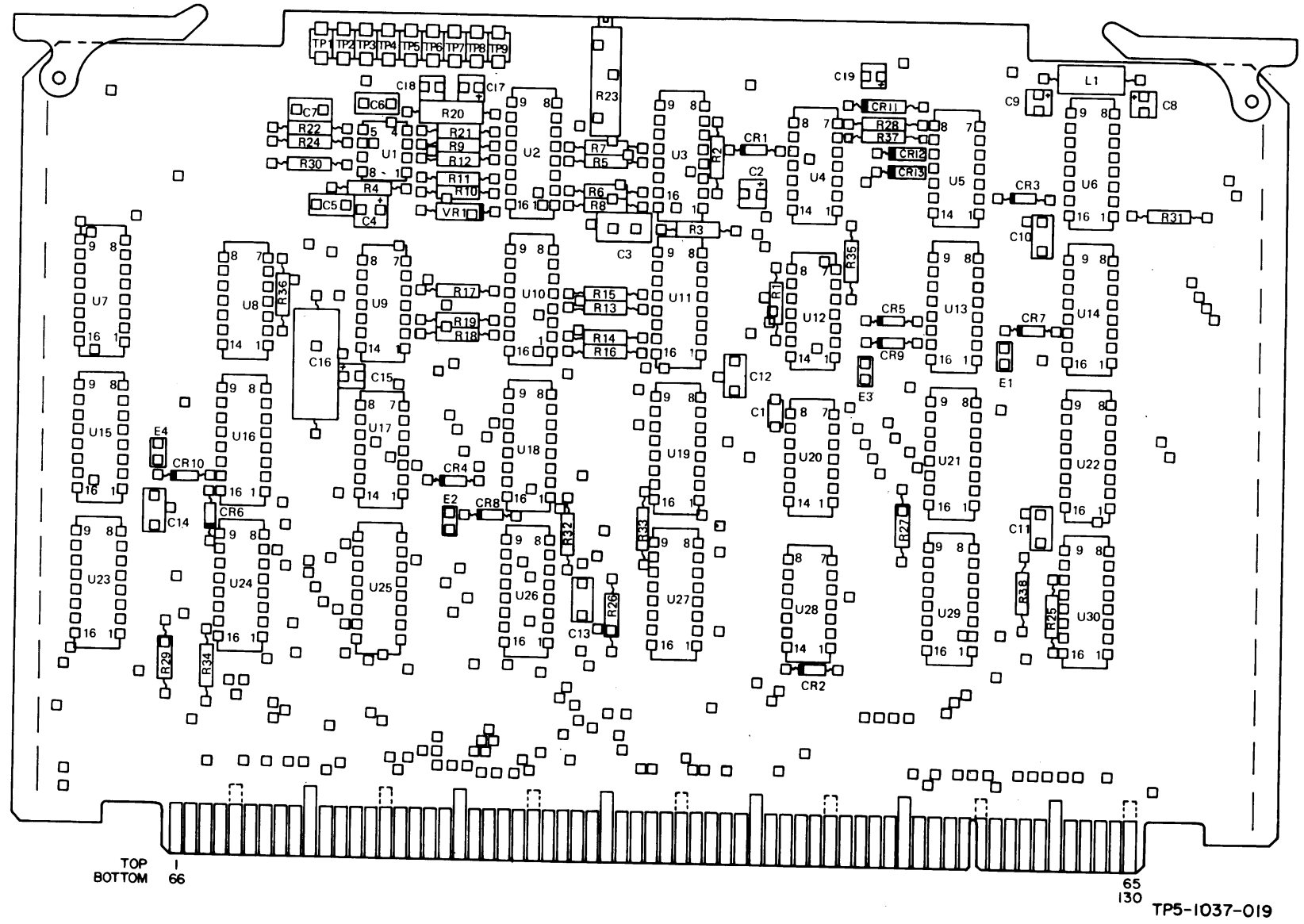
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 7. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Parallel output	635-0752-001	REV J
Parallel output	635-0752-002	REV K



Parallel Output, Schematic Diagram
Figure 7 (Sheet 1 of 8)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	PARALLEL OUTPUT 635-0752-001		A
	635-0752-002		B
CR1-CR10	SEMICOND DEVICE, 1N4454	353-3644-010	
CR11-CR13	SEMICOND DEVICE, 1N4454	353-3644-010	B
C1	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C2	CAPACITOR, FXD, ELCTLT, 0.47μF, 20%, 35V	184-9102-330	
C3	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C4	CAPACITOR, FXD, ELCTLT, 15μF, 20%, 15V	184-9102-130	
C5-C7	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C8, C9	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C10-C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	
C16	CAPACITOR, FXD, PLSTC DIEL, 1μF, 10%, 50V	933-1081-200	
C17	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V (A4)	184-9102-350	A
C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V (A1)	913-3279-200	A
C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	B
C19	CAPACITOR, FXD, ELCTLT, 1μF, 20%, 35V	184-9102-350	B
L1	COIL, RF, 1000μH	240-2540-000	
R1-R3	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R4	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R5	RESISTOR, FXD, FILM, 10.2kΩ, 1%, 1/8W	705-3605-480	
R6	RESISTOR, FXD, FILM, 11kΩ, 1%, 1/8W	705-1046-000	
R7	RESISTOR, FXD, FILM, 11.8kΩ, 1%, 1/8W	705-3605-510	
R8	RESISTOR, FXD, FILM, 13kΩ, 1%, 1/8W	705-3605-530	
R9	RESISTOR, FXD, FILM, 14kΩ, 1%, 1/8W	705-1051-000	
R10	RESISTOR, FXD, FILM, 15.4kΩ, 1%, 1/8W	705-1053-000	
R11	RESISTOR, FXD, FILM, 17.4kΩ, 1%, 1/8W	705-3605-590	
R12	RESISTOR, FXD, FILM, 19.6kΩ, 1%, 1/8W	705-1058-000	
R13	RESISTOR, FXD, FILM, 22.1kΩ, 1%, 1/8W	705-3605-640	
R14	RESISTOR, FXD, FILM, 26.1kΩ, 1%, 1/8W	705-1064-000	
R15	RESISTOR, FXD, FILM, 30.9kΩ, 1%, 1/8W	705-3605-710	
R16	RESISTOR, FXD, FILM, 38.3kΩ, 1%, 1/8W	705-1072-000	
R17	RESISTOR, FXD, FILM, 51.1kΩ, 1%, 1/8W	705-1078-000	
R18	RESISTOR, FXD, FILM, 76.8kΩ, 1%, 1/8W	705-3605-900	
R19	RESISTOR, FXD, FILM, 154kΩ, 1%, 1/8W	705-1101-000	
R20	RESISTOR, FXD, FILM, 309kΩ, 1%, 1/8W	705-3601-230	
R21, R22	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R23	RESISTOR, VAR, 10kΩ, 10%, 3/4W	382-0012-290	
R24	RESISTOR, FXD, FILM, 1kΩ, 1%, 1/8W	705-0996-000	
R25, R26	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R27	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	A
R27	RESISTOR, FXD, CMPSN, 0.10MΩ, 10%, 1/4W	745-0821-000	B
R28-R35	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	
R36	RESISTOR, FXD, CMPSN, 0.33MΩ, 10%, 1/4W	745-0839-000	
R36	RESISTOR, FXD, CMPSN, 68kΩ, 10%, 1/4W, (A2)	745-0815-000	A
R36	RESISTOR, FXD, CMPSN, 0.68MΩ, 10%, 1/4W (A3)	745-0851-000	A
R36	RESISTOR, FXD, CMPSN, 0.68MΩ, 10%, 1/4W	745-0851-000	B
R37	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0857-000	B
R38	RESISTOR, FXD, CMPSN, 1MΩ, 10%, 1/4W	745-0851-000	B
TP1	JACK, TIP, BRN	360-0484-070	
TP2	JACK, TIP,RED	360-0484-020	
TP3	JACK, TIP, ORN	360-0484-050	
TP4	JACK, TIP, YEL	360-0484-060	
TP5	JACK, TIP, GRN	360-0484-040	
TP6	JACK, TIP, BLU	360-0484-080	
TP7	JACK, TIP, VIO	360-0484-090	
TP8	JACK, TIP, GRA	360-0484-100	
TP9	JACK, TIP, WHT	360-0484-010	
U1	INTEGRATED CKT, MC1458P1	351-1071-070	
U2	MOS, ANLG MXR, F4051PC	351-8227-010	
u3	INTEGRATED CKT, MC14528BCP	351-8421-020	
U4	INTEGRATED CKT, MC14011CP	351-8159-040	
U5	INTEGRATED CKT, F4013BPC	351-8159-110	
U6	INTEGRATED CKT, CD4094BE	351-8346-010	
U7	MOS, ANLG MXR, F4051PC	351-8227-010	
U8	MICROCIRCUIT, CD4047AE	351-8200-020	
U9	INTEGRATED CKT, MC14071BCP	351-8287-010	
U10	MOS, ANLG MXR, F4051PC	351-8227-010	
U11	INTEGRATED CKT, F4049BPC	351-8159-210	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
U12	INTEGRATED CKT, MC14070BCP	351-8407-010	
U13-U16	INTEGRATED CKT, CD4094BE	351-8346-010	
U17	INTEGRATED CKT, F4013BPC	351-8159-110	
U18, U19	INTEGRATED CKT, CD4094BE	351-8346-010	
U20	INTEGRATED CKT, F4013BPC	351-8159-110	
U21-U27	INTEGRATED CKT, CD4094BE	351-8346-010	
U28	INTEGRATED CKT, MC14081BCP	351-8287-030	
U29, U30	INTEGRATED CKT, CD4094BE	351-8346-010	
VR1	SEMICOND DEVICE, 1N752A (A4)	353-2712-000	
VR1	SEMICOND DEVICE, 1N751A	353-2710-000	A
VR1	SEMICOND DEVICE, 1N751A	353-2710-000	B

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Added C18, 0.1μF	REV C and above.
A2	Changed R36 from 330 kΩ to 68 kΩ,	REV D and above.
A3	Changed R36 from 68 kΩ to 680 kΩ.	REV F and above.
A4	Removed C17, 1μF, electrolytic from junction of R20 and U18-11 (+) to ground (-). Changed VR1 from 1N752A (5.6 V) to 1N751A (5.1 V).	REV J and above.

The preceding modification history effectivities apply only to the 635-0752-001. Preceding modifications are included in all 635-0752-002 cards.

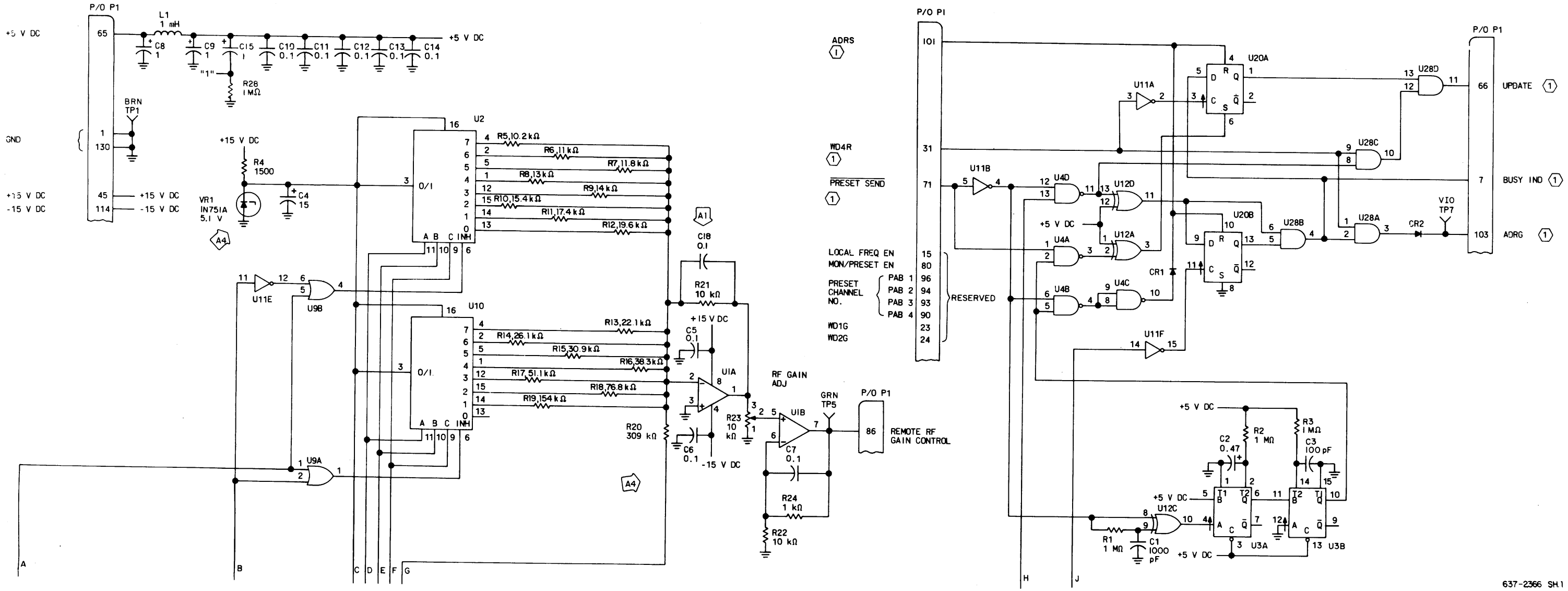
Parallel Output, Schematic Diagram
Figure 7 (Sheet 2)

POWER AND GROUND CONNECTIONS

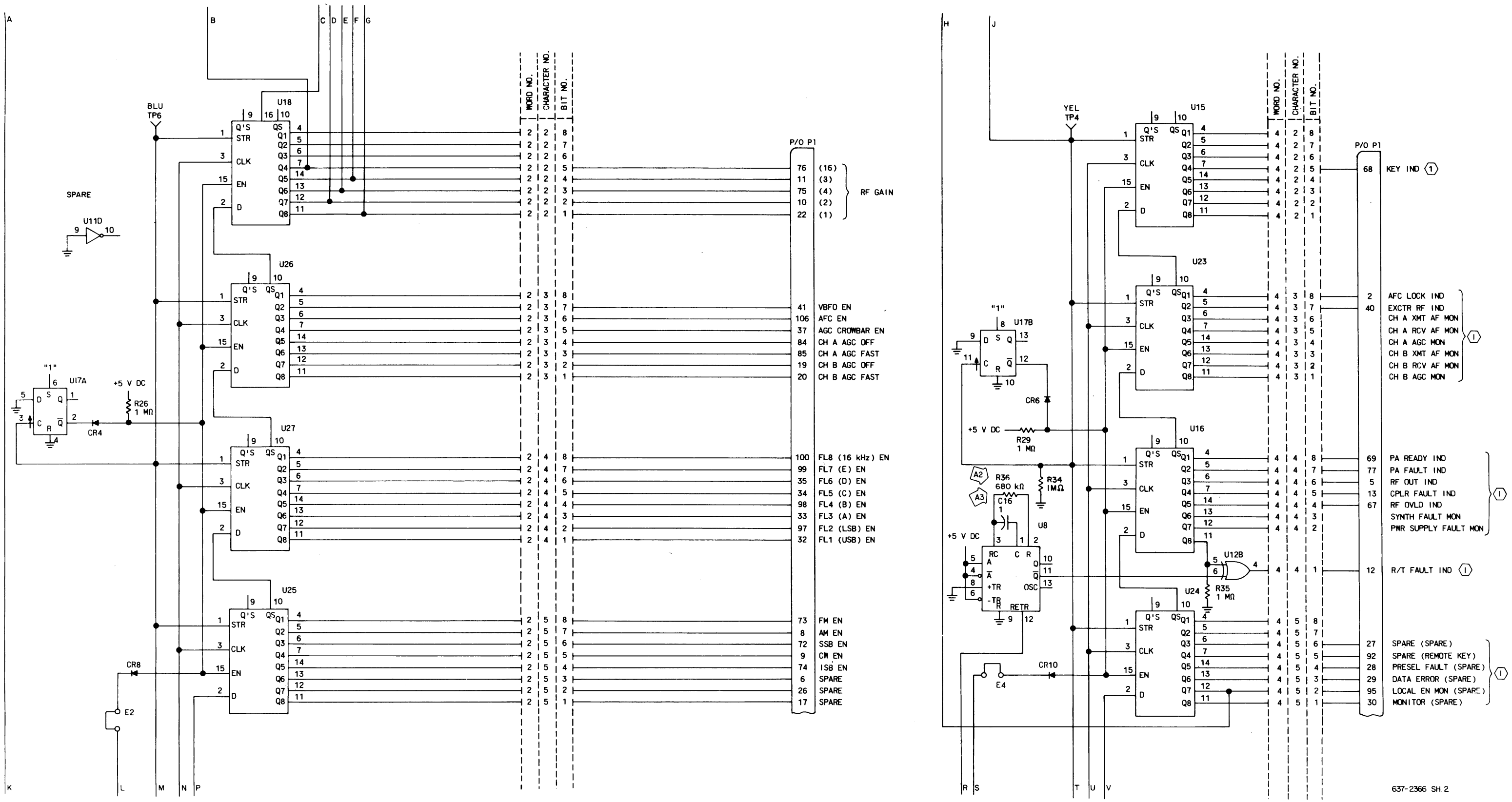
U NO.	TYPE	POWER (V DC)	
		+5	GND
U1	MC1458P1		
U2, U7, U10	F4051PC	16	8,7
U3	MC4528BCP	16	8
U4	MC4011CP	14	7
U5, U17, U20	F4013BPC	14	7
U6, U13–U16, U18, U19, U21–U27, U29, U30	CD4094BE	16	8
U8	CD4047AE	14	7
U9	MC4071BCP	14	7
U11	F4049BPC	1	8
U12	MC4070BCP	14	7
U18	MC4081BCP	14	7

NOTES:

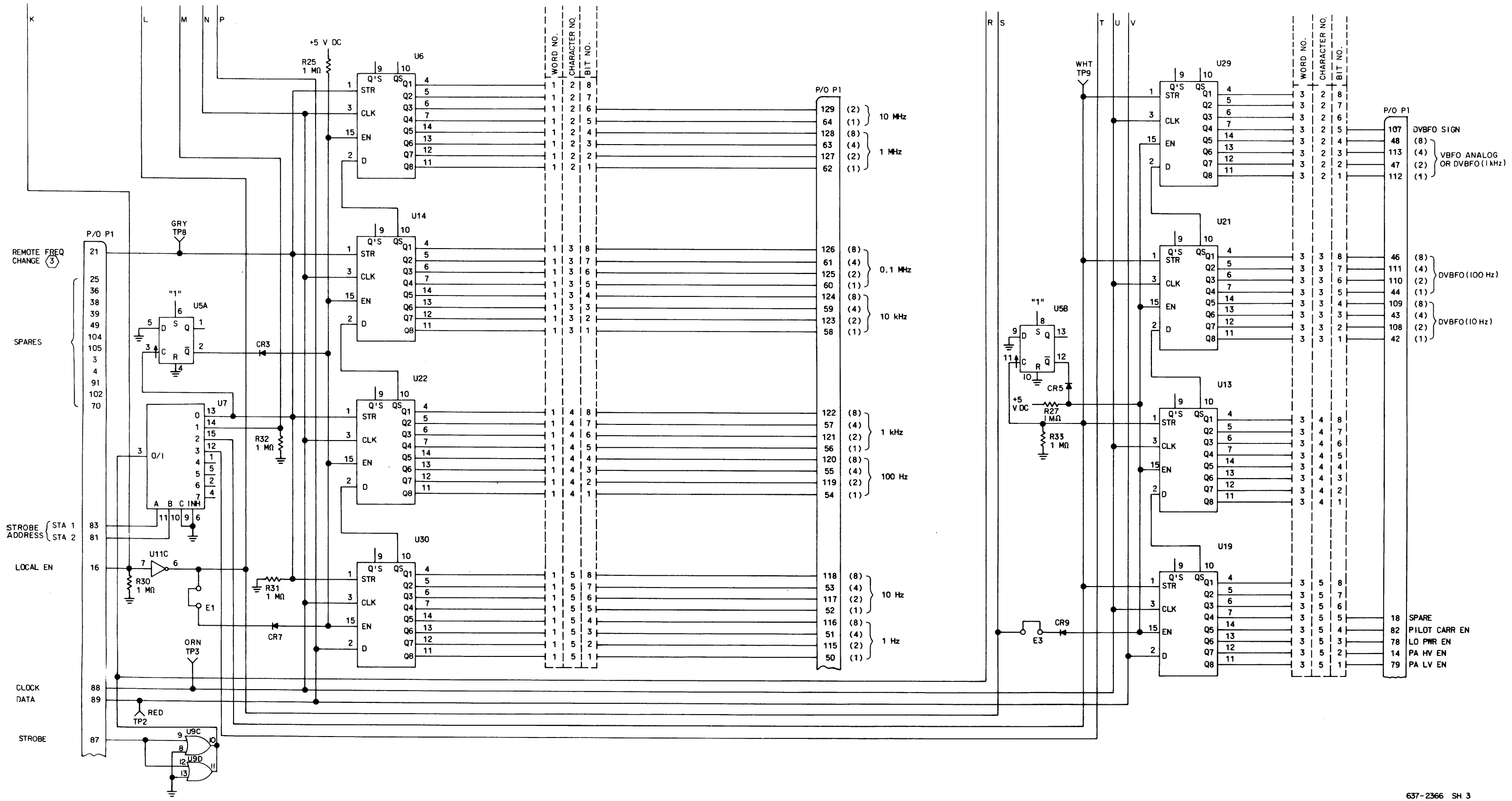
1. THESE FUNCTIONS ARE ONLY APPLICABLE TO REMOTE CONTROL UNITS.
2. FUNCTIONS IN PARENTHESES ARE APPLICABLE TO REMOTE CONTROL UNITS, (RCVR, EXCTR, RCVR-EXCTR). FOR A REMOTE UNIT, CHARACTER NO. LABELS SHOULD BE CHANGED FROM 5 TO 2.
3. THESE FUNCTIONS ARE NOT APPLICABLE TO REMOTE UNITS.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND DIODES ARE TYPE 1N4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.



Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 3)



Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 4)



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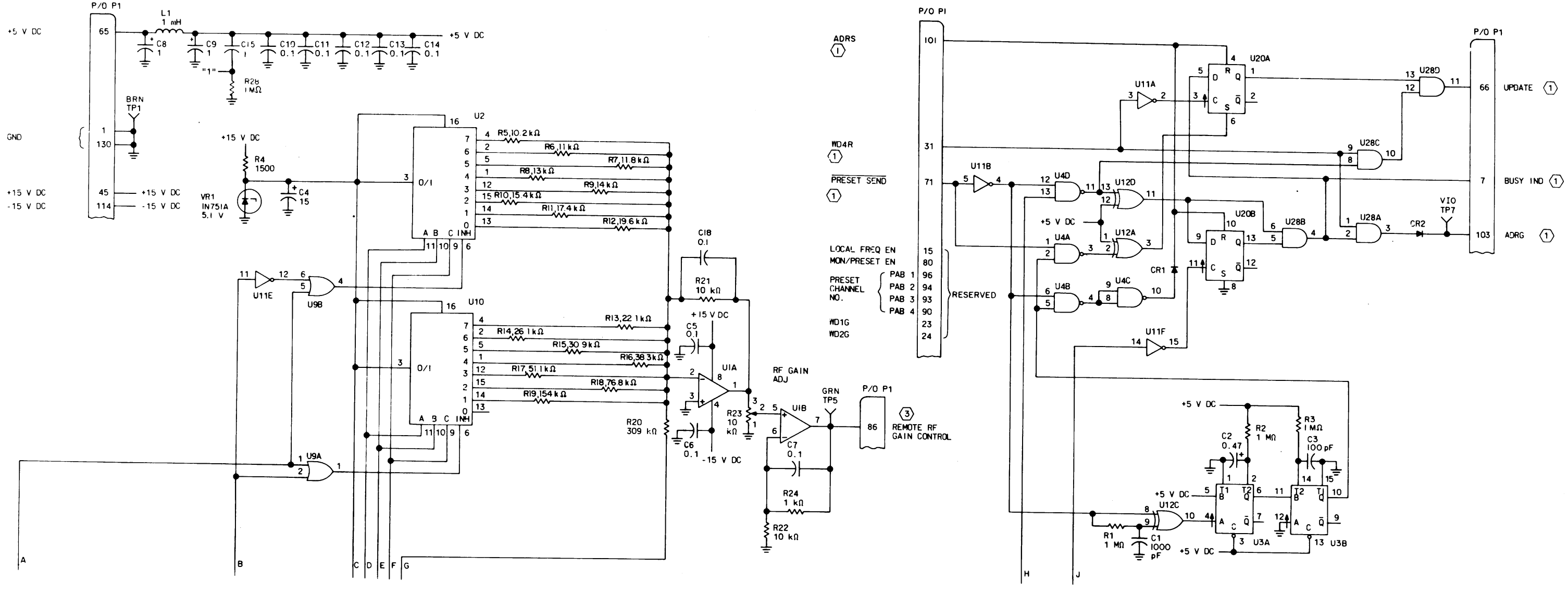
Parallel Output (635-0752-001), Schematic Diagram
Figure 7 (Sheet 5)

POWER AND GROUND CONNECTIONS

U NO	TYPE	POWER (V DC)	
		+5	GND
U1	MC1458P1		
U2, U7, U10	F4051PC	16	8,7
U3	MC14528BCP	16	8
U4	MC14011CP	14	7
U5, U17, U20	F4013BPC	14	7
U6, U13-U16, U18, U19, U21-U27, U29, U30	CD4094BE	16	8
U8	CD4047AE	14	7
U9	MC1407IBCP	14	7
U11	F4049BPC	1	8
U12	MC14070BCP	14	7
U18	MC14081BCP	14	7

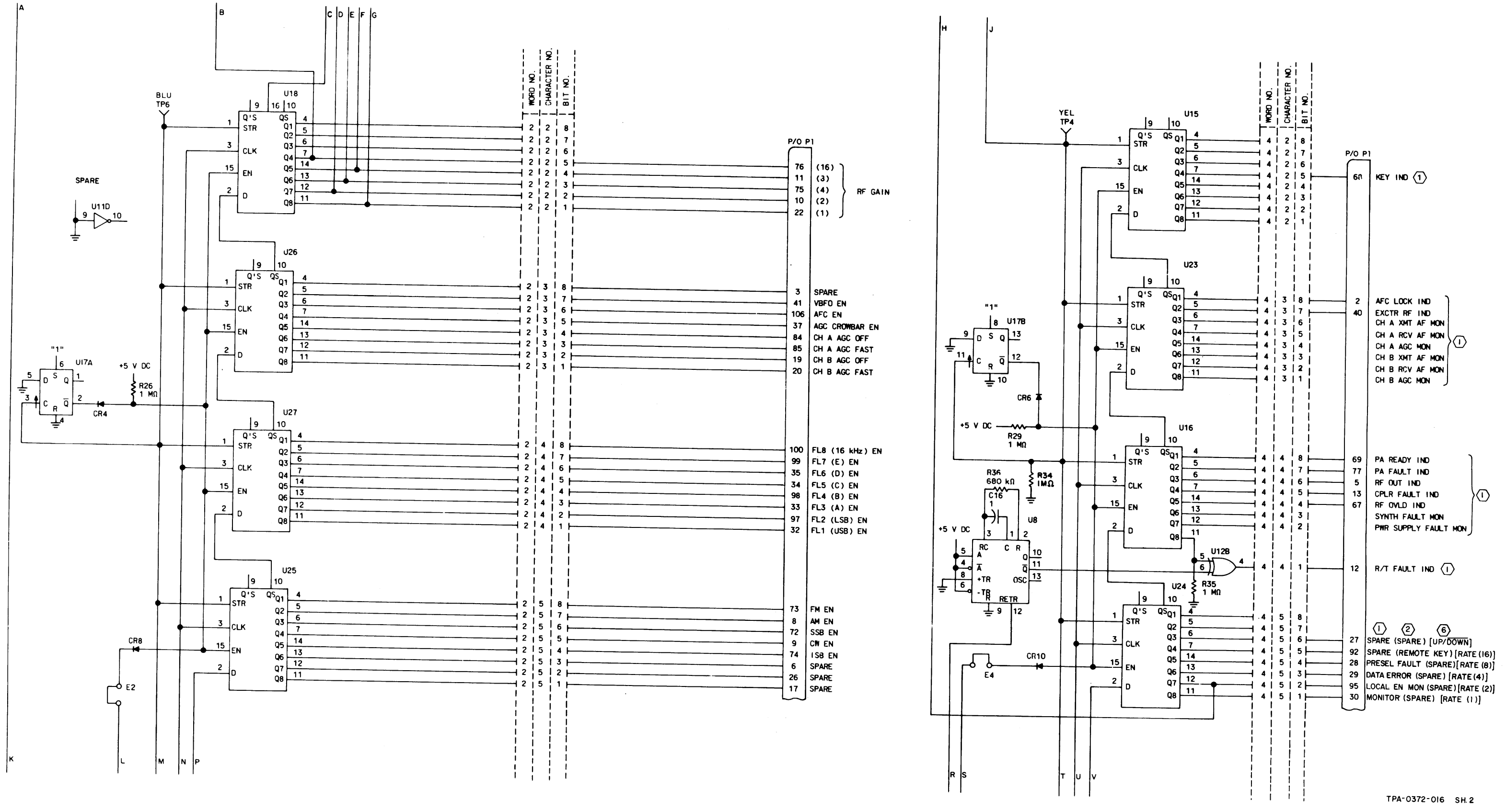
NOTES:

1. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR CONTROL, EXCTR CONTROL, AND RCVR-EXCTR CONTROL.
2. FUNCTIONS IN PARENTHESES ARE APPLICABLE TO RCVR, EXCTR, AND RCVR-EXCTR FOR A EXCTR, CHARACTER NO. LABELS SHOULD BE CHANGED FROM 5 TO 2.
3. THESE FUNCTIONS ARE APPLICABLE ONLY TO RCVR, EXCTR, AND RCVR-EXCTR.
4. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND DIODES ARE TYPE IN4454.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
6. FUNCTIONS IN BRACKETS [ ] ARE APPLICABLE ONLY TO 8515-( ) RCVR.
7. NONSTANDARD ABBREVIATIONS
   CH = CHANNEL
   EN = ENABLE

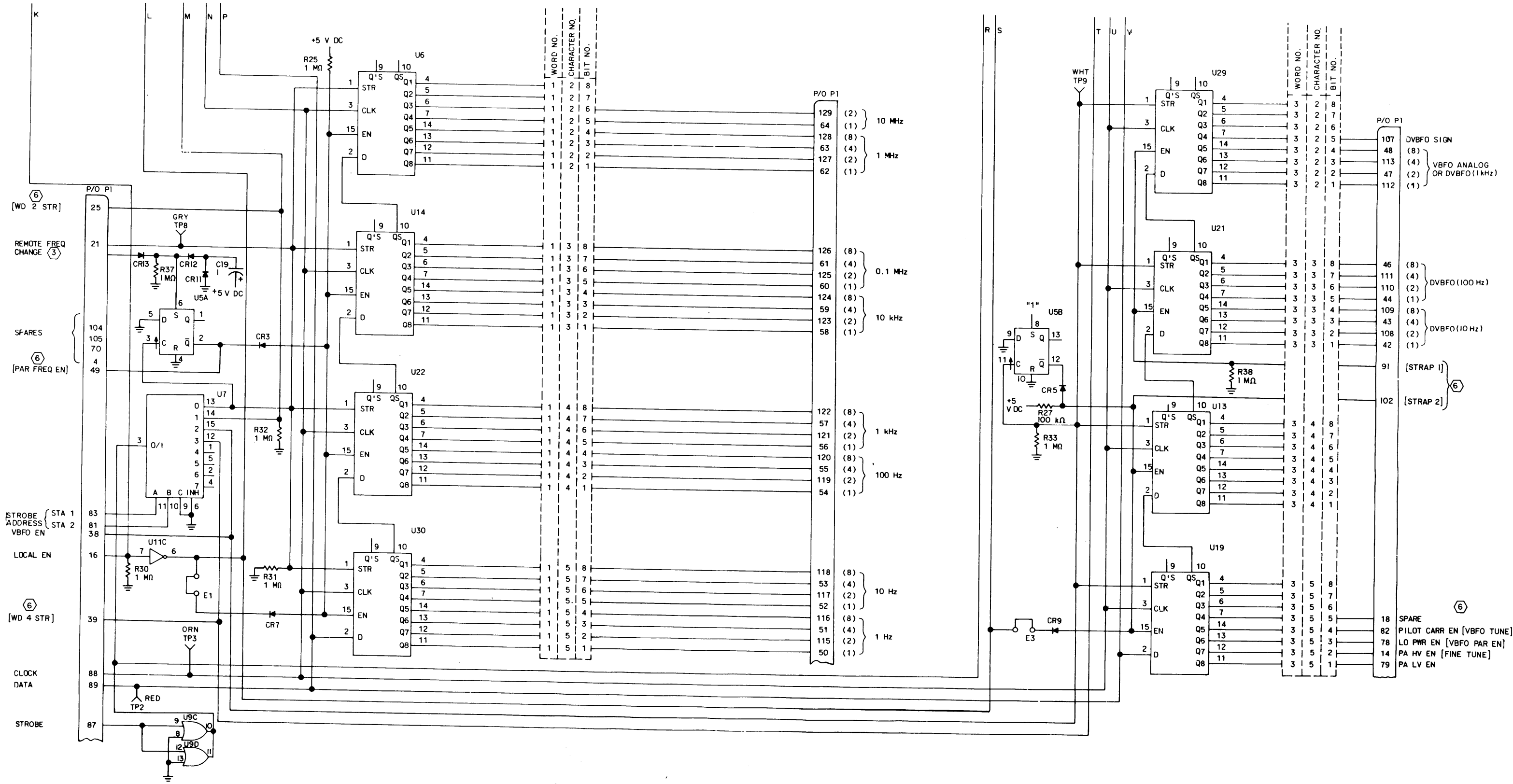


TPA-0372-016 SH.1

Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 6)



Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 7)



TPA-0372-016 SH. 3

Parallel Output (635-0752-002), Schematic Diagram
Figure 7 (Sheet 8)